

# Diagnostic Simulation of Sequential Circuits Using Fault Sampling

Srikanth Venkataraman<sup>†</sup>

W. Kent Fuchs<sup>‡</sup>

Janak H. Patel<sup>†</sup>

<sup>†</sup> Coordinated Science Laboratory, University of Illinois, Urbana, IL 61801

<sup>‡</sup> School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907

## Abstract

This paper describes a technique to accelerate diagnostic fault simulation of sequential circuits using fault sampling. Diagnostic fault simulation involves computing the indistinguishability relationship between all pairs of modeled faults. The input space is the set of all pairs of modeled faults, thus making the simulation computationally intensive. The diagnostic simulation process is accelerated by considering a sub-space of the input space that is obtained using fault sampling. Results on performance speedup and diagnostic resolution loss are provided for the ISCAS 89 benchmark circuits.

## 1 Introduction

The aim of *fault location* or *diagnosis* is to locate device failures. For diagnosis, test sets need to distinguish between as many faults as possible. Efficient generation of diagnostic test vectors requires a fast diagnostic simulator capable of determining the diagnostic capability of a given test set. Recent developments in diagnostic fault simulation have provided significant speedups [1, 2]. However, the complexity and the size of the problem requires considerable further performance gains before very large circuits can be evaluated. This paper describes an approach to speed up the diagnostic fault simulation of sequential circuits using fault sampling. The diagnostic simulation process is accelerated by considering a sub-space of the input space. The two key questions of speed up and accuracy of the diagnostic measures are addressed. The sampling process is intended to determine the diagnostic quality of a test set. However, it does not identify if a specific pair of faults are distinguished.

During fault simulation of a circuit from an unknown state, a good or faulty sequential circuit can produce a 0, 1 or X on each primary output for each test vector input, where X is an unknown value whose actual binary value depends on the initial state of the machine. If fault simulation indicates that

---

This research was supported in part by Defense Advanced Research Projects Agency (DARPA) under contract DABT 63-96-C-0069, by the Semiconductor Research Corporation (SRC) under grant 95-DP-109, by the Office of Naval Research (ONR) under grant N00014-95-1-1049, and by an equipment grant from Hewlett-Packard.

a fault  $f_i$  produces an output of 0 and another fault  $f_j$  produces an output of 1 on the same primary output for the same input vector, then the faults  $f_i$  and  $f_j$  are said to be distinguished. However, if a fault  $f_i$  produces an output of 0 or 1 and another fault  $f_j$  produces an output of X, then the faults  $f_i$  and  $f_j$  may possibly not be distinguished. Therefore, the pessimistic assumption is typically made that an output of 1 or 0 is indistinguishable from an output of X.

*Diagnostic Power (DP)* is the fraction of faults that are fully distinguished [3]. A fault is fully distinguished if the test set distinguishes it from every other fault in the fault list. *Diagnostic Expectation (DE)* [4] is the average size of the list of faults indistinguishable from any fault, given that all faults are equally likely to occur.

*Diagnostic fault simulation* is the process of determining these measures. Diagnostic fault simulation for sequential circuits by Rudnick et al. [5] uses a distinguishability matrix. The distinguishability matrix is an  $f$ -by- $f$  matrix, where  $f$  is the number of faults. An entry of 1 indicates that the two faults specified at the intersection of the row and column are distinguished by some sequence of test vectors in the test set. It requires  $O(f^2)$  space, and the time complexity is  $O(v \cdot o \cdot f^2)$ , where  $v$  is the number of vectors in the test set,  $o$  the number of outputs in the circuit and  $f$  the number of faults. It is obvious that the computational requirements increase considerably with the increasing number of simulated faults. Recently a diagnostic fault simulator for stuck-at faults in sequential circuits was developed that is both time- and space-efficient [2]. The representation is different from earlier work in that it does not explicitly store the indistinguishability relationship between all pairs of faults but represents the indistinguishability relationship between classes of faults. Each fault is present in only one of the classes.

Although sequential diagnostic fault simulation has made important performance gains, it still needs significant CPU time to complete the entire diagnostic simulation for the largest benchmark circuits. *Fault Sampling* [6, 7, 8] has been proposed as a technique that reduces the cost of fault simulation by simulating only a random sample of faults. However, this strategy cannot be directly applied to diagnostic fault simulation since the indistinguishability relationship

19980312 027

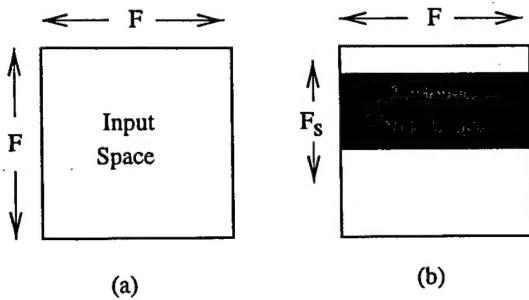


Figure 1: Input Space and The Sampled Sub-Space

between pairs of faults needs to be determined. Chakravarty [9] proposed a sampling technique for diagnostic simulation by sampling the equivalence classes. This technique cannot be directly used to sample the indistinguishability classes for sequential circuits since a fault may be present in multiple indistinguishability classes.

In this paper a sampling technique to perform diagnostic fault simulation of sequential circuits is proposed. The input space for diagnostic fault simulation is the set of all pairs of faults ( $F \times F$ ), where  $F$  is the set of all modeled faults. The sampling technique uses a sub-space ( $F_s \times F$ ) of the input space, where  $F_s$  is a set of sampled faults. This is illustrated in Figure 1. Sampling is performed by maintaining the sets of faults indistinguishable from each of the sampled faults. The sampling procedure identifies classes of faults that need to be maintained to determine these sets. The rest of the classes are dropped to speed up the simulation. The variance in the estimation due to sampling is also investigated.

## 2 Diagnostic Fault Simulation

In the following the diagnostic fault simulation procedure [2] is summarized. First the definitions and concepts essential to understanding the simulation are given.

**Definition 1** Two faults  $f_i$  and  $f_j$  are indistinguishable with respect to a test set  $T$ , if for every primary output and every input vector, either one (or both) of the output values of  $f_i$  or  $f_j$  is an  $X$ , or both the output values are not  $X$  but are the same.

**Definition 2** Two faults  $f_i$  and  $f_j$  are diagnostically equivalent with respect to a test set  $T$ , if for every primary output and every input vector, output values of  $f_i$  and  $f_j$  are the same. Here an  $X$  response is considered a different response from a 1 or a 0 response.

**Definition 3** A diagnostic equivalence class is a set of faults such that every pair of faults in the class is diagnostically equivalent by definition 2.

Table 1: Output Responses of an Example Circuit

Test vec.	Good ckt,	f1	f2	f3	f4	f5	f6	f7
v1	0xx	1xx	0x1	x1x	0x1	0xx	1xx	0x1
v2	x01	1xx	01x	x10	11x	x01	0xx	0x1

Definition 2 defines an equivalence relation over the set of faults  $F$ , and partitions  $F$  into sets of diagnostic equivalence classes. Each fault  $f_i \in F$  is present in only one diagnostic equivalence class. The faults within a diagnostic equivalence class cannot be distinguished by the given test set. However, these faults may not be equivalent in the boolean algebraic sense. However, definition 1 does not define an equivalence relation. A fault  $f_i \in F$  may be present in more than one indistinguishability class.

**Definition 4** An indistinguishability class is a set of faults such that every pair of faults in the class is indistinguishable by definition 1.

Table 1 gives the output responses of an example circuit with 3 primary outputs, 7 faults and 2 test vectors. The good and 7 faulty circuits are considered. The diagnostic fault simulation procedure can be explained using the notion of a *diagnostic tree*. A *diagnostic tree* is a connected, directed acyclic graph. A level in a diagnostic tree corresponds to one simulated test vector, while an edge in the tree corresponds to one set of distinct primary output values after the corresponding vector is simulated. Each node represents a *diagnostic equivalence class*. The diagnostic tree for the example circuit of Table 1 can be seen in Figure 2.

It is possible for two faults in two different diagnostic equivalence classes to be indistinguishable due to the  $X$  values generated during sequential circuit simulation starting from an unknown state. Such faults and their diagnostic equivalence classes are said to be *potentially distinguished*. This is represented using a *potentially distinguished pointer* between the two classes. For example, in Table 1, fault ( $f_3$ ) with a response  $X1X$ , and faults ( $f_2, f_4, f_7$ ) with a response  $0X1$  on test vector  $v_1$ , cannot be declared as distinguished

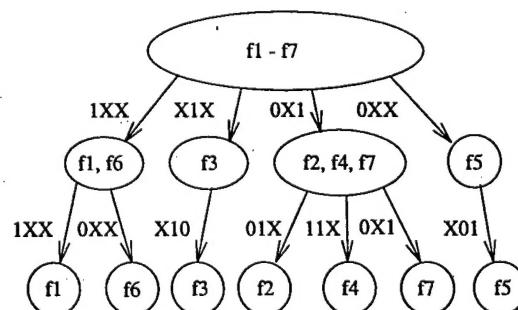


Figure 2: Diagnostic Tree for the Example Circuit

as there is no primary output with a response of 1 for one class and 0 for the other.

The diagnostic simulator simulates the test vectors and generates new diagnostic equivalence classes and potentially distinguished pointers between these classes corresponding to each new test vector. Figure 3 illustrates the diagnostic simulation process. The diagnostic measures are then computed as follows. The  $DP$  is computed as

$$DP = \frac{(\# \text{of uniquely distinguishable faults})}{(\text{Total } \# \text{ of faults})} \quad (1)$$

The  $DE$  is computed as

$$DE = \sum_{\forall \text{ faults } f} \frac{\# \text{ of faults indistinguishable from } f}{\text{total } \# \text{ of faults}} \quad (2)$$

During diagnostic fault simulation based on three-valued logic, if a fault  $f_1$  has a response  $X$  and a fault  $f_2$  has a response 1 (or 0) on the same output, then we cannot distinguish  $f_1$  and  $f_2$  with certainty. The pessimistic assumption made is that the two faults are indistinguishable [5]. Measures based on this assumption are *pessimistic measures*. As opposed to this, *optimistic diagnostic measures* make the assumption that the response  $X$  is different from a 1 or 0, i.e., faults with a response  $X$  are considered to be distinguished from faults with a response 1 or 0. The *pessimistic measures* and *optimistic measures* are the lower and upper bound of the actual diagnostic capability of a test set.

### 3 Sampling Technique

Consider the distribution of the number of faults indistinguishable from each fault  $f_i$  in the set of modeled faults  $F = \{f_1, f_2, \dots, f_N\}$ . Figure 4(a) shows an example distribution. Here  $I_i$  refers to the set of faults indistinguishable from fault  $f_i$  (including the fault  $f_i$ ). The diagnostic fault simulator implicitly represents this distribution in the diagnostic equivalence classes and potentially distinguished pointers as shown in Figure 4(b).

This distribution (with finite population size  $N$ ) induces a probability distribution function  $P(X)$ , which is defined in

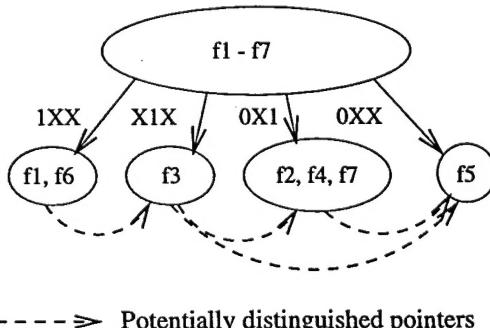
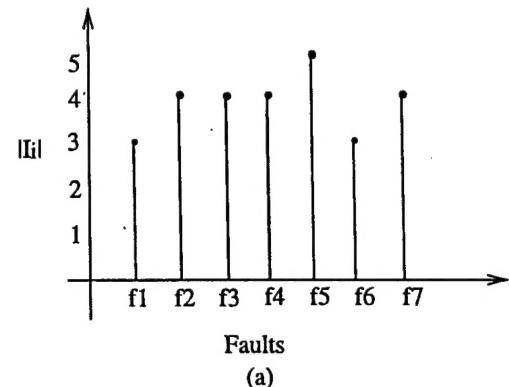


Figure 3: Diagnostic Fault Simulation



(a)



$$I_3 = \{f_1, f_3, f_5, f_6\}, |I_3| = 4$$

(b)

Figure 4: Distribution of Indistinguishable Faults

Equation 3. Here  $|S|$  refers to the cardinality of the set  $S$ . The random variable  $X$  is the value of  $|I_j|$  obtained by picking a fault  $f_j$  at random from the set of modeled faults  $F$ . The expected value  $\mu = E(X)$  of this random variable  $X$  is the *diagnostic expectation* of the test set as shown by Equation 4.

$$P(X = i) = \frac{|\{f_j : |I_j| = i\}|}{N} \text{ for } 1 \leq i \leq N \quad (3)$$

$$\begin{aligned} E(X) &= \sum_{i=1}^N X_i P(X_i) = \frac{\sum_{i=1}^N |I_i|}{N} \\ &= \text{Diagnostic Expectation (DE)} \end{aligned} \quad (4)$$

Consider the random variable  $Y$  defined by Equation 5. The probability distribution function of  $Y$  is given in Equation 6. The expected value of this random variable  $E(Y)$  is the *diagnostic power* of the test set as shown in Equation 7.

$$Y(f_i) = \begin{cases} 1 & \text{if } |I_i| = 1 \\ 0 & \text{if } |I_i| \neq 1 \end{cases} \quad (5)$$

$$P(Y = 1) = \frac{|\{f_i : |I_i| = 1\}|}{N} \quad (6)$$

$$E(Y) = \sum_{i=1}^N Y_i P(Y_i) = \text{Diagnostic Power (DP)} \quad (7)$$

A simple random sample of size  $n$  is picked without replacement from the set of  $N$  modeled faults. The sample mean

given by  $\bar{X} = \frac{1}{n}(X_1 + \dots + X_n)$  can be used as an estimator for the value of the diagnostic expectation. Similarly, the sample mean given by  $\bar{Y} = \frac{1}{n}(Y_1 + \dots + Y_n)$  can be used as an estimator for the value of the diagnostic power. The expected value of  $\bar{X}$ ,  $E(\bar{X}) = E(X)$ , and the expected value of  $\bar{Y}$ ,  $E(\bar{Y}) = E(Y)$ . Thus,  $\bar{X}$  and  $\bar{Y}$  are consistent estimators for diagnostic expectation and diagnostic power respectively. The  $X_i$  and  $Y_i$  values can be obtained from the sets of faults indistinguishable from each of the  $n$  sampled faults.

### 3.1 Sampled Diagnostic Simulation

Although conceptually simple, sampling cannot be done directly during diagnostic simulation of sequential circuits for two reasons. The set of faults indistinguishable from a given fault is not explicitly maintained. Further, the complete distribution is obtained only after processing all test vectors. The diagnostic simulation procedure is modified as follows. After each test vector is processed to generate new equivalence classes and potentially distinguished pointers, the faults indistinguishable from each of the sampled faults are determined. For each of the sampled faults, the following computation is performed. The faults in the diagnostic equivalence classes containing the sampled fault are indistinguishable from the sampled fault. Further, faults in equivalence classes that are potentially distinguished from this class are also indistinguishable from the sampled fault. All such equivalence classes, their corresponding faults and potentially distinguished pointers, are marked. The unmarked equivalence classes and their corresponding faults are distinguished from all the sampled faults. Thus, the unmarked equivalence classes, their corresponding faults, and the unmarked potentially distinguished pointers are not required for computing the sets of faults indistinguishable from each of the sampled faults, and can hence be dropped during simulation. This speeds up the simulation process.

Figure 5 illustrates the sampled diagnostic simulation. Consider the set of modeled faults  $F = \{f_1, f_2, \dots, f_7\}$ . Figure 5(a) shows the distribution of the faults indistinguishable from each of the faults in  $F$ . The sampled set is  $F_s = \{f_1, f_3\}$ . One level of the diagnostic tree is shown in Figure 5(b). The classes  $\{f_1, f_6\}$  and  $\{f_3\}$  contain the sampled faults and are hence marked. The class  $\{f_5\}$  is potentially distinguished from  $\{f_3\}$  and is hence marked. The potentially distinguished pointers from class  $\{f_1, f_6\}$  to class  $\{f_3\}$ , and from class  $\{f_3\}$  to class  $\{f_5\}$  are marked. The class  $\{f_2, f_4, f_7\}$  and the potentially distinguished pointer from class  $\{f_2, f_4, f_7\}$  to class  $\{f_5\}$  are unmarked and can be dropped from the simulation.

### 3.2 Sampling Variance

In the case of simple random sampling without replacement from a finite population of size  $N$ , the variance of the sampling distributions  $\bar{X}$  and  $\bar{Y}$  are given by Equation 8 [10].

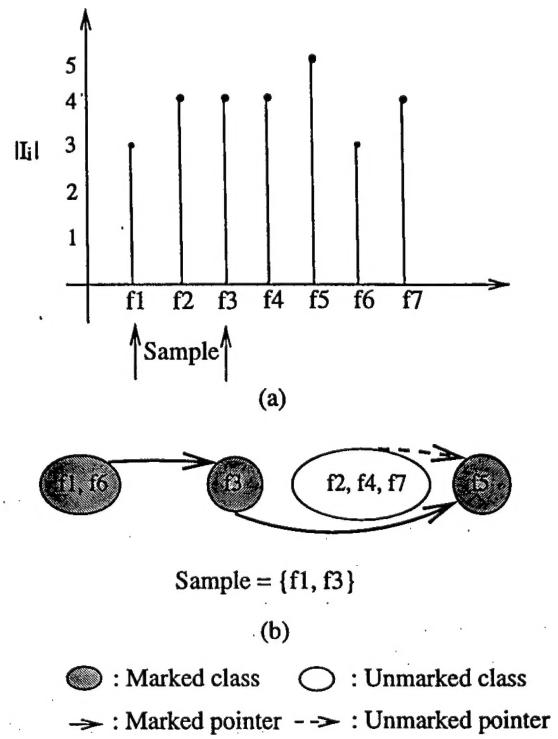


Figure 5: The Sampling Process

Here,  $\sigma_X^2$  and  $\sigma_Y^2$  are the variance of the distributions of the random variables  $X$  and  $Y$  respectively. The variance of the sampling distributions  $\bar{X}$  and  $\bar{Y}$  are a measure of the expected estimation errors for diagnostic expectation and diagnostic power respectively.

$$var(\bar{X}) = \frac{\sigma_X^2}{n} \frac{N-n}{N-1} \text{ and } var(\bar{Y}) = \frac{\sigma_Y^2}{n} \frac{N-n}{N-1} \quad (8)$$

$\sigma_Y^2$  can be expressed as a function of DP. From Equations 5 and 7 it follows that  $E(Y^2) = E(Y) = DP$ . Hence  $\sigma_Y^2 = E(Y^2) - \mu^2 = DP(1 - DP)$ . Thus the variance of the estimated diagnostic power is given by Equation 9.

$$var(\bar{Y}) = \frac{\sigma_Y^2}{n} \frac{N-n}{N-1} \approx \frac{1}{n} DP(1 - DP)(1 - \frac{n}{N}) \quad (9)$$

The accuracy of the estimate depends on three factors: the absolute size of  $n$ , the relative size of  $n/N$ , and the value of DP. In a manner similar to that in the analysis by Agrawal [6], the estimated DP ( $\bar{Y}$ ), for large  $N$ , can be approximated by a normal distribution with mean  $\mu_Y = E(\bar{Y}) = DP$ , and variance  $\sigma_{\bar{Y}}^2 = var(\bar{Y})$ . For large values of  $N$  ( $N \gg n$ ),  $n/N$  can be approximated to 0. This is true for the realistic case of large circuits with large values of  $N$  and small sample sizes. The accuracy now depends on the size of  $n$  and value of DP.

For a confidence level of 99.7 percent, the estimated diagnostic power is in the interval  $[DP - 3\sigma_{\bar{Y}}, DP + 3\sigma_{\bar{Y}}]$ . The estimation error is almost certainly bounded by  $3\sigma_{\bar{Y}}$ . Thus, from Equation 9, the maximum error is given by  $e_{max} = 3 \times \sqrt{DP(1 - DP)/n}$ . The worst case occurs when  $DP = 50\%$ . For this case a sample size of  $n=1000$  ensures a maximum error of 5% [11].

## 4 Experimental Results

The sampling technique was implemented on top of the diagnostic fault simulator (RAPSIM) [2]. The sampled diagnostic fault simulator was run on a SUN SPARCstation 20 with 64MB of memory for the ISCAS89 benchmark circuits [12] and a synthesized circuit piir8 which is an 8-bit IIR DSP filter. The diagnostic capabilities of the test set generated by HITEC [13] were evaluated. All large benchmark circuits were considered. Partial scan versions of s13207, s15850, s38417 and s38584 were used to get deterministic test sets with reasonable fault coverage. Strictly undetected faults (faults that have the same response as the good circuit for the test set) were removed using fault simulation with fault dropping. These faults form one large diagnostic equivalence class. The rest of the faults were considered for the full and sampled versions of the diagnostic fault simulator. Table 2 gives the execution time for full diagnostic fault simulation ( $n=all$ ) and the speedup for varying sample sizes (500, 1000, 1500). Note that the largest circuit takes about 5 hrs of CPU time for full diagnostic fault simulation. The execution time for the sampled simulation is the average of ten executions performed using different seeds for the random number generator. As expected, the simulation time required decreases with smaller values of  $n$ . For the three largest circuits, a sample size of 1000 faults speeds up the simulation by a factor of 6 on the average.

Table 3 shows the diagnostic measures for the full diagnostic simulation ( $n=all$ ) and the estimated diagnostic measures for varying sample sizes (500, 1000, 1500). The estimated diagnostic measures are the average of ten simulations. The error between the exact and estimated diagnostic measure is expressed as a percentage. As expected, the error decreases with increasing sample size. Note that the error for  $DP$  is less than 5% for a sample of 1000 faults, as predicted. The error for  $DP$  power is about 1% on the average for a sample size of 1000 faults. The error for  $DE$  is about 2% on the average for a sample size of 1000 faults. The sampled diagnostic simulation also has lower memory requirements than full diagnostic simulation.

## 5 Summary

A sampling technique for diagnostic fault simulation of sequential circuits has been described. The sampling technique uses a sub-space of the input space. Sampling is

Table 2: Execution Time Speedup by Sampling

Circuit	Test Vec.	Faults	Sample Size	Average Exec. Time (s)	Speedup
s13207s	2753	6766	n=all	2081.55	
			n=500	820.2	2.5
			n=1000	1122.8	1.8
s15850s	2119	8453	n=all	1902.4	
			n=500	565.5	3.3
			n=1000	738.2	2.5
piir8	347	16613	n=all	1178.8	
			n=500	368.2	3.2
			n=1000	510.0	2.3
			n=1500	602.1	1.9
s35932	383	34417	n=all	4099.5	
			n=500	446.8	9.1
			n=1000	561.8	7.3
			n=1500	695.2	5.9
s38417s	3499	21586	n=all	14195.8	
			n=500	2390.7	5.9
			n=1000	3541.0	4.0
			n=1500	4060.2	3.5
s38584s	3002	31528	n=all	18217.0	
			n=500	2178.8	8.3
			n=1000	2964.2	6.1
			n=1500	3747.3	4.9

performed by maintaining the sets of faults indistinguishable from each of the sampled faults. The sampling procedure identifies classes of faults that need to be maintained to determine these sets. Experimental results show that the method obtains good speedups by considering a fixed sample of about 1000 faults and using a simple random sample. The procedure results in a small loss of accuracy in the resulting diagnostic measures. The variance in the estimation is investigated theoretically and experimentally. For a small sample size of 1000 faults the error in the estimation of the diagnostic measures is about 2% on the average.

## Acknowledgements

The authors gratefully acknowledge their discussions with Sreejit Chakravarty.

## References

- [1] J. M. Jou and S.-C. Chen, "A Fast and Memory-Efficient Diagnostic Fault Simulation for Sequential Circuits," in *Proc. of the IEEE/ACM Intl. Conf. on CAD*, pp. 723-726, Nov. 1994.
- [2] S. Venkataraman, I. Hartanto, W. K. Fuchs, E. M. Rudnick, S. Chakravarty, and J. H. Patel, "Rapid Diagnostic Fault Simulation of Stuck-at Faults in Sequential

Table 3: Diagnostic Measures for HITEC Test Vectors

Circuit	Sample Size	Pessimistic				Optimistic			
		DP (%)	% Error	DE	% Error	DP (%)	% Error	DE	% Error
s13207s	n=all	37.0		3.75		45.6		3.18	
	n=500	37.9	2.4	3.83	2.1	44.6	2.1	3.27	2.8
	n=1000	36.6	1.0	3.65	2.6	44.7	1.9	3.13	1.5
s15850s	n=all	41.5		3.81		47.5		3.30	
	n=500	42.3	1.9	3.77	1.0	48.9	2.9	3.25	1.5
	n=1000	42.1	1.4	3.79	0.5	48.2	1.4	3.28	0.6
piir8	n=all	10.1		8.12		10.1		8.11	
	n=500	10.6	4.9	7.92	2.4	10.6	4.9	7.93	2.4
	n=1000	10.2	0.9	8.10	0.2	10.2	0.9	8.10	0.2
	n=1500	10.2	0.9	8.08	0.4	10.2	0.9	8.08	0.4
s35932	n=all	0.0		5.08		33.5		1.90	
	n=500	0.0		4.85	4.5	32.6	2.6	1.95	2.6
	n=1000	0.0		4.91	3.3	33.1	1.1	1.93	1.0
	n=1500	0.0		5.14	1.1	33.2	0.9	1.92	1.5
s38417s	n=all	57.3		3.58		61.3		3.22	
	n=500	59.2	3.3	3.27	8.6	62.3	1.6	3.42	6.2
	n=1000	55.8	2.5	3.67	2.5	60.3	1.6	3.39	5.2
	n=1500	56.3	1.7	3.53	1.3	60.5	1.3	3.13	2.7
s38584s	n=all	65.6		2.54		70.6		2.29	
	n=500	64.7	1.3	2.45	3.5	70.0	0.8	2.42	5.6
	n=1000	65.8	0.3	2.67	4.8	70.1	0.7	2.21	3.4
	n=1500	65.8	0.3	2.61	2.7	70.3	0.4	2.31	0.8

- Circuits Using Compact Lists," in *Proc. of the Design Automation Conf.*, pp. 133–138, June 1995.
- [3] P. Camurati, D. Medina, P. Prinetto, and M. S. Reorda, "A Diagnostic Test Pattern Generation Algorithm," in *Proc. of the IEEE Intl. Test Conf.*, pp. 52–58, Sept. 1990.
- [4] P. G. Ryan, W. K. Fuchs, and I. Pomeranz, "Fault Dictionary Compression and Equivalence Class Computation for Sequential Circuits," in *Proc. of the IEEE/ACM Intl. Conf. on CAD*, pp. 508–511, Nov. 1993.
- [5] E. M. Rudnick, W. K. Fuchs, and J. H. Patel, "Diagnostic Fault Simulation of Sequential Circuits," in *Proc. of the IEEE Intl. Test Conf.*, pp. 178–186, Oct. 1992.
- [6] V. D. Agrawal, "Sampling Techniques for Determining Fault Coverage in LSI Circuits," in *Journal of Digital Systems*, pp. 189–202, Fall 1981.
- [7] R. L. Wadsack, "Design Verification and Testing of the WE32100 CPUs," *IEEE Design and Test of Computers*, vol. 1, pp. 66–75, Aug. 1984.
- [8] W. Daehn, "Fault Simulation Using Small Fault Samples," *Journal of Electronic Testing: Theory and Applications*, vol. 2, pp. 191–203, 1991.
- [9] S. Charkravarty, "A Sampling Technique for Diagnostic Fault Simulation," in *Proc. of the VLSI Test Symposium*, pp. 192–197, Apr. 1996.
- [10] B. W. Lindgren, *Statistical Theory*. Macmillan Publishing Co., Inc., 1976.
- [11] M. Abramovici, M. A. Breuer, and A. D. Friedman, *Digital System Testing and Testable Design*. AT&T Bell Laboratories and W. H. Freeman and Company, 1990.
- [12] F. Brglez, D. Bryan, and K. Kozminski, "Combinational Profiles of Sequential Benchmark Circuits," *IEEE Intl. Symp. on Circuits and Systems*, pp. 1929–1934, May 1989.
- [13] T. Niermann and J. H. Patel, "HITEC : A Test Generation Package for Sequential Circuits," in *Proc. of the European Design Automation Conf.*, pp. 214–218, Feb. 1991.

# PURDUE UNIVERSITY



SCHOOL OF ELECTRICAL AND  
COMPUTER ENGINEERING  
WEST LAFAYETTE, IN 47907-1285 U.S.A.

W. KENT FUCHS  
HEAD

March 2, 1998

Colin E. Wood  
ONR 312  
Office of Naval Research  
Ballston Centre Tower One  
800 North Quincy Street  
Arlington, VA 22217-5660

COPY

Dear Dr. Wood:

Enclosed is a copy of the final version of the paper (citation below) concerning research supported in part by the Department of the Navy and managed by the Office of the Chief of Naval Research under grant N00014-95-1-1049:

S. Venkataraman, J. Patel, and W. K. Fuchs, "Diagnostic Simulation of Sequential Circuits Using Fault Sampling," *Proceedings of the Eleventh IEEE International Conference on VLSI Design*, Jan. 1998, pp. 476-481.

This material is covered under Distribution Statement A (Approved for Public Release: Distribution is Unlimited).

We appreciate your support of this research.

Sincerely,

A handwritten signature in black ink, appearing to read "W. Kent Fuchs".

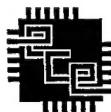
W. Kent Fuchs  
Professor and Head

Enclosure: manuscript

cc:      Administrative Grants Officer (Chicago IL)  
          Director, Naval Research Laboratory (Washington DC)  
          Defense Technical Information Center (Ft. Belvoir VA)

WKF:jc

1285 Electrical Engineering Building  
email: fuchs@purdue.edu



Phone: (765) 494-3539  
Fax: (765) 494-3544